EVALUATION OF STRAIN SOURCES IN BOND AND ETCHBACK SILICON-ON-INSULATOR

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Abstract

The incorporation of strain is inherent in the manufacture of bond and etchback silicon-on-insulator (BESOI) substrates. In this paper, the principal sources of strain are identified and the magnitude of the strain is estimated. The strain sources discussed include dopant (boron) induced lattice contraction of the etchstop layer, differential thermal expansion, and interfacial microroughness at the time of bonding. Reduction or elimination of SOI layer degradation from some of these strain sources is possible.

1. Introduction

Silicon-on-insulator (SOI) is a versatile technology that allows complete dielectric isolation of adjacent microelectronic devices. The SOI substrate is a laminar composite structure generally made up of three discrete layers. The silicon in which devices are built is the top layer, and is referred to as the device layer, or simply the SOI. Below the SOI is an insulating layer, usually SiO\textsubscript{2}, which is known as the buried oxide. The buried oxide separates the SOI from a bulk silicon wafer, generally referred to as the handle wafer.

Strain in an SOI layer may originate from several sources. The most important are the differential thermal expansion (DTE) of silicon and silicon dioxide, micro-roughness of the silicon dioxide surface at bonding, and the dopant induced strain incorporated into the epitaxial layers. Although strains due to doping can largely be eliminated by a codoping procedure, other strain sources cannot be eliminated. Because bond and etchback silicon-on-insulator (BESOI) is a laminar multi-layered structure made by contacting surfaces which are not ideally flat, residual strain from local deformation must be
expected. The thermal expansion of Si and SiO\textsubscript{2} are significantly different. This is another source of deformation. The following sections describe the crystal quality of SOI, and the effect of various strain sources is presented.

2. Fabrication

BESOI wafer fabrication is illustrated in Fig. 1. The process begins with the formation of a buried $p^+$ etchstop layer in a silicon substrate. A double epitaxial deposition is commonly used to generate the required structure. The $p^+$ etchstop layer is deposited first, followed by a layer which will ultimately become the device layer of the SOI substrate. An effective etchstop layer requires a $p^+$ concentration above $7 \times 10^{19}$ cm\textsuperscript{-3}. Boron concentrations in this range cause contraction of the silicon lattice. The associated stress in the etchstop layer increases with boron concentration and layer thickness. Since the device layer silicon is epitaxially grown directly on the etchstop layer, the expectation is that stress induced lattice defects in the etchstop layer will degrade the crystal quality of the device layer. Yeh and Joshi [1] proposed compensating for the boron induced lattice contraction by adding germanium to the etchstop layer. The usefulness of this procedure has been demonstrated [2, 3]. Optimum ratios of Ge:B have been reported for codoped silicon epitaxial etchstop layers and we have also determined this ratio.

Samples for this study were made using prime grade, $<100>$, 100 mm diameter substrates. Epitaxial etchstop and device layers were deposited in a
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single wafer atmospheric pressure reactor at 1140°C. The epitaxial wafers had a 40 nm oxide grown on them, and a thicker oxide, either 1 or 2 microns was grown on another group of prime grade wafers, commonly referred to as handle wafers or substrate wafers. The wafers were wet cleaned and contacted together at room temperature, then annealed at 850°C in oxygen. The bonded wafer pairs were then thinned down by lapping and chemical etching to form the desired SOI structure. Detailed descriptions of the BESOI process may be found in the literature [4, 5].

We have found that oxidation of both wafers prior to bonding is necessary to maintain the desired doping characteristics. Spreading resistance probe measurements indicate the presence of a p-type impurity at the Si-SiO₂ interface when a high resistivity bare silicon wafer is bonded to an oxidized wafer. The p-type contamination is pervasive in fabrication environments, and adsorbs on the bare silicon surface. During oxidation the impurities segregate preferentially into the SiO₂, and have a negligible effect on the resistivity of the silicon. If bare silicon is bonded without prior oxidation the positive charge on the surface is trapped in the silicon near the interface with the insulating oxide.

3. Experiments and results

3.1. The epitaxial etchstop

The epitaxial etchstop was characterized in order to establish the relationship between doping and defect density. Evaluating the etchstop layer before bonding allowed the stress produced by the epitaxial deposit to be determined prior to the formation of the SOI structure. The chemical composition of a series of etchstop layers was determined via SIMS. These etchstop layers were all 3.5 microns thick, with a peak boron concentration of $1 \times 10^{20} \text{cm}^{-3}$. The germanium content was varied from zero to above $1.5 \times 10^{21} \text{cm}^{-3}$. Even at the higher concentrations the incorporation of boron and germanium is virtually non-competitive. With all source gas flows constant (except the Ge supply, which was 10% GeH₄ in H₂) the boron content in each sample remained constant as the germanium content was increased. The concentration of both dopants was found to be constant throughout the epi layer.

To detect etchstop defects samples were angle lapped and decorated using a modified Shimmell etch. As the germanium content was increased, a range was defined where no defects were detected. Dislocations were absent for Ge: B ratios from 4.5:1 through 12:1. Outside this range an orthogonal grid of misfit dislocations was present (Fig. 2).
Fig. 2. Photomicrograph of epitaxial etchstop layers. Misfit dislocations are revealed in the sample (a) doped only with boron; the layer compensated with germanium (b) has no visible dislocations.

Fig. 3. A series of x-ray rocking curves made on epitaxial etchstop layers. Samples had a fixed concentration of boron in the epitaxial layer while the germanium concentration was varied. The peak separation is an indication of epilayer strain. (a) Ge = 0; (b) Ge = 4 × 10^{20} \text{ cm}^{-3}; (c) Ge = 8 × 10^{20} \text{ cm}^{-3}; (d) Ge = 14 × 10^{20} \text{ cm}^{-3}.
X-ray data was collected using a high resolution diffractometer. The system consists of a rotating anode x-ray generator (copper anode), a four reflection Bartels–Dummond type monochromator (using Ge <220> reflections) and a goniometer having omega scan capability. For each layer studied two pairs of bond measurements were made using omega scans over the (004) which are almost parallel to the sample surface, and the (444) which are inclined to the sample surface by about 54.7 degrees.

The effect of increasing the Ge : B ratio of etchstop layers may be seen in Fig. 3. This series of (004) x-ray rocking curves indicates that both the peak position and full width at half maximum (FWHM) of the etchstop layer are affected by the germanium level. In each diffractogram the peak at 34.564 degrees is from the substrate, while the other peak arises from the epitaxial etchstop layer. The variation in the height of the peaks is because of thickness differences in the etchstop layer. The displacement of the epi layer Bragg peaks is due to a uniform epilayer strain. Based on the superposition of peaks (substrate and epitaxial etchstop) the optimal compensation occurs at a Ge : B ratio of 9 : 1. This value is greater than that obtained by Maszara [2], and less than the value measured by Herzog, Cspregi and Seidel [3]. Figure 3 also indicates that the FWHM for each of the germanium codoped layers is lower than for the etchstop layer doped with boron alone, but greater than the substrate. Actual values ranged from 22.4 arc-sec. for layers doped with boron alone, down to 18 to 19 arc-sec. for germanium codoped samples. Close examination of Fig. 3d reveals an unexpected additional peak, much smaller than the two primary peaks. Multiple peaks for epitaxial layers with boron concentrations of $1 \times 10^{20}$ cm$^{-3}$ or more were reported by Holloway and McCarthy [6]. They concluded that peak multiplicity arose from a lateral variation in the coherence of the epitaxial layer with the substrate.

Calculations of the relaxed lattice constant of codoped epitaxial layers were made to determine the optimum compensation ratio. To determine the lattice constants reported, data were corrected for refraction. The 004 bond measurements were used to calculate the (004) d-spacing, and the silicon lattice constant $a$ perpendicular to the layer. The 444 Bond measurements were used to calculate the d-spacing of the (444). It was assumed that each layer might be tetragonally distorted; $a$ perpendicular and $d_{444}$ were used to calculate a parallel, the lattice constant parallel to the sample surface. Figure 4 is a plot of relaxed lattice constant as a function of Ge : B ratio. Dislocation free silicon with a total impurity content of less than $1 \times 10^{16}$ cm$^{-3}$ has a lattice constant of 5.43106 angstroms [7]. The codoped epitaxial layers are fully strain compensated, with a lattice constant equal to undoped dislocation free silicon at a...
Fig. 4. Measured values of the relaxed lattice constant of codoped epitaxial etchstop layers as a function of Ge: B ratio.

Ge: B ratio of 9: 1. This is in agreement with the ratio which we determined by measurement of the Bragg peak displacement.

3.2. Evaluation of the SOI material

The influence of codoping is apparent when finished SOI structures are viewed under an inspection lamp ($\lambda = 630$ nanometers). This type of lamp is used in processing to monitor the etching of the $p^+$ etchstop layer. Substrates which had etchstop layers doped with boron alone contain polygonized arrays of misfit dislocations, visible without using a decorative etch. The liquid etchants employed for BESOI manufacture will delineate the defects due to the locally increased etch rate associated with crystalline imperfections. Evidently the thermal excursions of the epi deposition process are sufficient to allow stress relief through plastic deformation of the layer. Samples appropriately codoped with germanium and boron were free of misfit dislocations when viewed under monochromatic light.

X-ray reflections from the SOI layer and the handle wafer were separable due to the silicon wafers being cut with the surface inclined to the $<001>$ by about 0.10 to 0.20 degrees. The FWHM of 004 rocking curves reflected
from the SOI layer was broader than those from the handle wafer. No global biaxial strain was detectable, within experimental error, after refraction corrections were made. The diffractometer used had a sensitivity in $\Delta d/d$ of approximately 1 part in 70,000, so stress levels in the silicon would have to be above $2 \times 10^7$ dynes cm$^{-2}$ to be detected.

Based upon the results of the etchstop layer evaluation described above it was determined that SOI substrates codoped with germanium at a ratio near 9:1 would produce the four most favourable x-ray results. However, in the SOI substrates measured, no improvement was seen as a result of Ge codoping. The final SOI structures clearly exhibit the effect of additional strain sources. Figures 5a, b demonstrate that there is no improvement in crystalline quality based on measurements of the lattice constant and FWHM of SOI structures due to codoping. Most values of $<004>$ FWHM on SOI were around 35 arc-sec., with one near 60 arc-sec. While the minimization of uniform epilayer strain via appropriate compensation eliminated the epilayer defects resulting from dopant induced lattice contraction, codoped samples did not produce narrower rocking curves. Our calculations indicate that a dislocation density of $1 \times 10^4$ cm$^{-2}$ will result in a broadening of less than 4 arc-sec. Clearly, crystalline defects are not the primary source of the FWHM broadening. The formation of the SOI structure introduces additional sources of nonuniform elastic strain, resulting in increased FWHM in the x-ray spectra.

Variations in the FWHM were shown to be unrelated to the presence or absence of dislocations in the epitaxial etchstop layer, however the cause was still unclear. Investigation of the bonding process revealed that variations in peak width occurred from wafer to wafer within a lot of bonded wafers rather than between lots bonded on different days. This suggests that variations in the oxidation process or cleaning prior to bonding are an unlikely source. Rocking curves are consistent at different sites on a given wafer, indicating that broadening is not the result of isolated micro-defects such as particles. While point defects such as stacking faults most commonly cause peak broadening, nonuniform strain resulting from micro-roughness of the wafer surfaces at bonding would also cause peak broadening. Interfacial microroughness at bonding is suspected as the principal source of peak broadening in our wafers because of the low density ($<10$ cm$^{-2}$) of dislocations found in the SOI layer of substrates made with appropriately compensated epitaxial etchstops after defect etching in modified Shimmel etch. Even samples with polygonized misfit defects visible optically did not produce poorer x-ray spectra, as would be expected if crystalline defects were the primary source of the peak broadening. Broadening of the SOI
Fig. 5. Measurements of the lattice parameter and FWHM of the SOI layer and the handle wafer in the vicinity of the buried oxide. The SOI layers are all doped to approximately $5 \times 10^{14}$ cm$^{-3}$ with boron, however, the etchstop layer used during fabrication was compensated with varying amounts of germanium.
device layer peak relative to the handle wafer was reported by Yamada et al. [8]. His group also found poor correlation between peak broadening and the density of observed crystalline defects.

3.3. The role of microroughness

Because of the poor correlation between visible defect density and x-ray peak broadening, elastic strain generated at the bond interface was suspected as the principal cause of the broadening. There are three modes of localized strain which may result from deformation of wafers at bonding: simple bending (with lateral strain), shearing motion, and thickness change (due to vertical stress). Only simple bending is significant for the case of SOI structures [8]. The impact of localized bending on the Bragg condition [9] may be expressed as:

\[ \Delta \theta \approx \left( \frac{\Delta d}{d} \right) \tan \theta + \Delta \phi + \Delta \theta' \]  

where \( \theta \) is the Bragg angle, \( d \) is the interplanar distance, \( \Delta d/d \) is the strain normal to the reflecting plane, and \( \phi \) is the inclination of the reflecting planes to the interface. The angular fluctuations of reflecting planes will also influence the x-ray diffraction. This is accounted for in the final term \( \Delta \theta' \), a constant which is related to the periodicity and amplitude of the interfacial microroughness.

Wafer deformation during bonding to accommodate both microscopic and macroscopic surface irregularities will generate local stress. The relation between surface morphology and deformation during bonding has been investigated [10]. The surface roughness of the prime wafers used as handle wafers as well as wafers with epitaxial layers was measured using scanning white light interferometry (SWLI). This data allowed the calculation of the degree of stress imparted to the SOI structures as a result of the accommodation of surface irregularities during bonding. Figure 6a is a typical three-dimensional surface profile, Fig. 6b indicates the amplitude of the surface topography as a function of spatial frequency, and Fig. 6c is a two-dimensional plot of surface height vs. distance. Taken together they reveal that the dominant component (i.e. greatest amplitude) has a spatial frequency of one to three millimeters. This variation at low spatial frequency is generally referred to as waviness. The mean surface waviness had an amplitude of 40 nm for epitaxial wafers and 27 nm for prime handle wafers. The amplitude of variations at higher spatial frequencies is more than an order of magnitude lower. The FWHM broadening for the \(<004>\) reflection caused by wafer surface irregularities (inclinations) at bonding was estimated. When the waviness of the SOI layer interface with the buried oxide has a spatial frequency of 2 mm and an amplitude of 40 nm the
peak broadening of 15–20 arc-sec. seems reasonable. This is at least four times greater than the broadening resulting from a dislocation density of $1 \times 10^4$ cm$^{-2}$ in the SOI layer.

The local stress caused by the deformation of the wafer surfaces at bonding can be estimated. Because the thickness, $t$, of the SOI layer is much smaller than the wafer diameter, a model based on the bending of a uniformly loaded circular plate may be used to calculate the stress due to local flattening of the rough surface [10]. Two cases for the plate model must be evaluated. In the
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first case the plate is clamped at the edge, and no edge movement is allowed. Thus the maximum stress is present at the perimeter of the plate, and is given by:

\[ \sigma_{\text{max}} = \frac{4Eht}{a^2(1 - u^2)} \]  \hspace{1cm} (2)

In the second case, the edge of the plate is supported but not clamped, the edge is free to move upon loading. In this case the highest stresses are at the centre of the plate, and may be expressed as:

\[ \sigma_{\text{max}} = \frac{2Eht(3 + u)}{a^2(5 + u)(1 - u)} \]  \hspace{1cm} (3)

where \( h \) represents the height difference between peaks and valleys on the wafer surface, \( a \) is \( \frac{\lambda}{\pi} \) of the spatial frequency of \( h \), \( t \) is the thickness of the SOI layer (1.5 microns in our case), and \( u \) is Poisson's ratio. The highest stress case will occur when surface asperities on the respective wafer surfaces are aligned. When epitaxial layers with a mean surface roughness of 40 nanometers are used to make BESOI wafers the stress predicted by eq. (2) is \( \approx 1.7 \times 10^6 \) dynes cm\(^{-2}\). Using eq. (3) the predicted stress is \( \approx 5.1 \times 10^5 \) dynes cm\(^{-2}\). Because some degree of edge movement of the SOI layer with respect to the bulk is likely, the true stress should lie somewhere between the two calculated values. The stress associated with microroughness is localized, and varies in sign with the amplitude fluctuations of the bond interface. Therefore, this stress sums to zero, or very nearly zero for large areas. Even the highest values for the localized stress due to microroughness as calculated above fall below the detection limit of our x-ray tool.

3.4. Evaluation of commercial SOI wafers

X-ray rocking curves of bonded SOI samples prepared by precision grinding and grinding followed by local area plasma thinning were also taken. These wafers were obtained commercially from two independent vendors [11, 12]. One of the manufacturers thins the SOI by precision grinding, the other used precision grinding followed by local plasma thinning. The samples made by precision grinding and grinding followed by plasma thinning had similar values of FWHM for the \( \{004\} \) reflection. Both were narrower than for the chemically thinned BESOI. A lower level of microroughness at the bond interface may be at least partially responsible for the narrower rocking curves found on these samples. Epitaxial layers are not used in the techniques based on precision grinding, so any increase in surface microroughness associated with the epi process is avoided. It is also noteworthy that other
investigators [10, 13] have reported lower values for the waviness of prime grade wafers used for SOI fabrication, ranging from ~2 to 13 nm, significantly less than the mean value of 27 nm for the handle wafers used for our BESOI material. If the commercial wafers used in the present work had a microroughness of the order of 8 nm, and the spatial frequency remained at 1 to 3 mm, a factor of 5 reduction in the nonuniform strain generated from this source would result. Therefore approaches which use ultra flat substrates without the need for epitaxial layers can be expected to produce SOI substrates that will have x-ray spectra with narrower FWHM.

4. Discussion

Because both the front and back surfaces of the handle wafer are oxidized to the same thickness before bonding and anneal, the strain resulting from the disparity in DTE between the insulating oxide and the silicon is balanced, and there is virtually no spherical deformation of the wafers due to bending strain relief. Removal of the back surface oxide results in significant warpage of the substrate. This has been verified experimentally via device fabrication on BESOI wafers. Warpage results from the different thermomechanical characteristics of the constituent layers; specifically the DTE between silicon and SiO₂. The stress introduced into the SOI layer may be calculated after measuring the overall warpage, provided that the layer thicknesses and physical characteristics of the constituent layers is known [14]. For the case of a 1.5 micron thick SOI layer with a 2.0 micron thermally grown buried oxide, on a 525 micron thick, 100 millimeter diameter silicon substrate the stress in the silicon is \( \approx 5 \times 10^7 \) dynes cm\(^{-2} \). This value is based on the assumption that nearly all of the 2 micron buried oxide is grown on the handle wafer prior to bonding. (This is done because thermal cycling of the epitaxial substrate must be kept to a minimum to preserve the sharp transition in doping between the etchstop and device epi layers.) Typically a 40 nm oxide on the epi wafer is sufficient to eliminate the presence of undesired p-type surface contaminant described earlier. While the calculated stress level in the device silicon layer increases as a result of strain relief when the SiO₂ is removed from the back of the handle wafer, the overall stress in the SOI substrate decreases. This results from the fact that the stress in the buried oxide is much higher than in the silicon and is significantly reduced through bending strain relief.

5. Conclusions

Various strain sources encountered in the production of BESOI have been described. Strain resulting from dopant induced lattice contraction can be
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eliminated by appropriate codoping. Strains induced by microroughness and DTE are inherent, because SOI is a laminar multilayered structure. Micro-roughness necessitates localized deformation of the surfaces during bonding, and localized inclinations of the silicon result. These are easily detectable with x-ray diffraction but cause relatively low levels of induced strain. Calculated values of induced strain resulting from microroughness are a factor of 20 below the induced strain in the silicon from DTE.

The high concentrations of boron necessary to form an etchstop layer result in the formation of misfit dislocations. The source of the strain which generates the dislocations is the size mismatch between boron and silicon. Dislocations can be eliminated if germanium is added to the etchstop layer along with boron. The optimum compensation occurs at a ratio of 9:1, Ge:B.

The stress imparted to the silicon as a result of DTE and interfacial microroughness are well within the elastic range of the material. It is believed that the non-uniform strain resulting from interfacial microroughness is largely responsible for x-ray peak broadening. Based on measurement of the surface microroughness of wafers prior to bonding we estimate a resultant broadening of 15 to 20 arc-sec. In contrast, the broadening due to the presence of misfit dislocations was determined to be less than 4 arc-sec. Although the broadening is easily detectable, the induced stress in the silicon resulting from microroughness is localized and small. Integrated circuit fabrication generates stresses orders of magnitude larger than those calculated for surface microroughness. It is unlikely that the induced stress from microroughness will affect integrated circuit processing. The largest stress present in compensated SOI originates from the DTE of the buried oxide relative to the silicon. It is important to match the thickness of the buried oxide with the oxide on the back surface of the substrate in order to minimize wafer warpage. Warpage resulting from significant thinning of the back surface oxide during processing will introduce bending strain to the SOI layer. When 2 micron thick buried oxides are used, wafer warpage can exceed 100 microns if the back surface oxide is removed, making integrated circuit processing virtually impossible. Therefore conservation of the back surface oxide throughout processing is required.

References


[12] Hughes Danbury Optical Systems, 100 Wooster Heights Road, Danbury, CT, USA.
