A new system of digital circuit blocks for industrial measuring and control equipment  

D. Gossel, G. Kaps and W. Schott

Introduction
The characteristic of digital information processing installations is that in their construction a small group of basic circuits is used, each of which occurs in large numbers. The group of basic circuits is called a system.

In order to enable designers to realize a given logical design without going into electronic details, several manufacturers have developed systems consisting of "And", "Or" and "Negation" circuit blocks as well as bistable circuits (flip-flops) for counting and storing purposes [1].

Although it should be possible to realize any logical design using such a system, circuit limitations must be considered, and extensive load tables limit the possibilities of combining the various blocks. The number of prohibited combinations increases with the number of different blocks, making the load tables more and more complicated. Amplifiers for decoupling purposes — e.g. P-N-P and N-P-N emitter followers — have to be used, although they have no logical function, and this is at variance with the original aim [2]. Consequently there are systems in which the total number of blocks required for a given problem bears no relation to the number that have a logic function. This influences not only costs, but also reliability, since an increase in the number of blocks also causes an increase in the failure rate.

Efforts have been made to avoid these difficulties by decreasing the number of basic circuits. Switching algebra provides a solution through the use of De Morgan’s formula [3]:

\[ x_1 + x_2 + \ldots + x_n = \bar{x}_1 \cdot \bar{x}_2 \cdot \ldots \cdot \bar{x}_n, \]
\[ x_1 \cdot x_2 \cdot \ldots \cdot x_n = \bar{x}_1 + \bar{x}_2 + \ldots + \bar{x}_n. \]

This formula gives the relationship between the AND and OR operation and the Negation. It may be seen from this that the one operation can always be replaced by the other together with the negation.

The NAND and NOR techniques often used at present go another step further. Here it is possible by using suitable combinations of the AND operation together with negation, or the OR operation together with negation, to make only one type of block suffice [4].

Fig. 1 shows the AND and OR operation realized with NAND- and NOR-blocks. Each NAND and NOR symbol represents one basic circuit containing at least one transistor together with resistors, capacitors and diodes.

A second advantage of using only one type of block for all logical circuits is that the load tables in the NAND and NOR systems reduce to one single load rule. It is only necessary to know how many NAND or NOR circuits can be reliably controlled by a previous NAND or NOR. There are no other forms of loading.

A serious disadvantage however is the large number of blocks to be used for certain operations. In order to realize an OR operation, one relatively expensive NAND block is necessary for each input (fig. 1a). The AND

Dipl.-Ing. D. Gossel, Dipl.-Ing. G. Kaps and Dipl.-Ing. W. Schott are research workers at the Hamburg laboratory of Philips Zentrallaboratorium GmbH.

[1] Editorial note: An article by E. J. van Barneveld, Philips ICOMA Division, Eindhoven, will be appearing shortly in this journal, describing another system of digital circuit blocks, designed for more universal use than the system presented here, and which is now being put into production by the ICOMA Division.
operation, however, can always be realized by two NAND blocks regardless of the number of inputs (within certain limits). This also holds true when only NOR blocks are used; but in this case AND and OR operations are exchanged (fig. 1b) [3].

The new building-block system

The new system of digital circuit blocks described in this paper can be regarded as an attempt to reach a good compromise between these two methods. One of the characteristics of the new system is the use of only two basic circuits, an active one, and a passive one. The active block contains a circuit in diode-transistor logic (DTL). With the logic convention chosen ("1" \( \equiv \) 12 V, "0" \( \equiv \) 0 V) this block works as a NOR circuit (fig. 2). The passive block is an AND circuit (also called an AND gate) with two inputs (fig. 3). The number of inputs can within wide limits be increased by means of additional diodes. Using the passive AND block it is not necessary to realize the AND operation with NOR blocks in the expensive way shown in fig. 1b.

This building-block system which is especially designed for industrial measurement and control purposes also has the following characteristics.

1. There are no emitter followers. Only one type of transistor and two types of diode are used.
2. A standardized voltage supply is used (\( \pm 12 \) V \( \pm 5\)%). This value is considered a good compromise between
   a) a high voltage, giving low sensitivity to interference and great freedom in combining various numbers and types of block — i.e. wide signal tolerances are permitted —, and
   b) a low voltage which suits the low maximum permissible voltage for available transistors and gives low dissipation.
3. The maximum switching frequency is 80 kc/s, the maximum counting frequency 30 kc/s. (In some cases the maximum counting frequency may be 80 kc/s.) In industrial applications the electronic circuits are mainly used together with moving parts which have a certain mass. Experience here has shown that, resolving power (accuracy) and speed call for a counting frequency of 10 kc/s at the most. A frequency of 30 kc/s is thus adequate for quite extreme requirements.
4. Asynchronous or synchronous modes of operation are optional. For simple problems involving low-speed counting, the well-known asynchronous method may be used. Here for example a bistable circuit is triggered by a previous one which also has to supply the switching energy. The maximum counting rate is determined by the sum of the switching times of all stages and thus decreases with an increasing number of stages. The maximum load per stage is much reduced in asynchronous counting techniques.

When somewhat higher demands are made, the synchronous counting mode is to be preferred because of its great advantages, although a few more blocks are needed. Here all the stages of a counting circuit receive switching pulses from a common clock-pulse generator. Each stage contains a separate signal input \( S \), and the voltage applied to this input determines whether or not a given clock pulse will trigger the circuit. This method has the following consequences.

a) The circuit is very insensitive to interference. As a result of the delaying effect of the pulse gate controlled via the \( S \) input, parasitic pulses in the signal line will only be able to cause incorrect switching if their duration is \( \geq 5 \mu s \) and their voltage-time integral is more than \( 60 \, \mu \)Vs, and the clock pulse is received more than \( 5 \mu s \) after the start of a parasitic pulse. Under normal conditions it is unlikely that these three conditions will be satisfied simultaneously. In practice therefore there will be almost no interference.

b) The various stages are not subjected to a dynamic load of any significance, since the triggering energy is supplied by the common clock-pulse generator. With the exception of the clock-pulse line, which should be as short and of as low capacity as possible, all signal lines are uncritical.

c) Unlimited use may be made of the maximum switching frequency. All stages which have to be triggered are prepared during the interval between two clock pulses, and are triggered by the next clock pulse received. The switching times of successive stages are not additive. No stringent demands are made for the rise time of the signal voltage at the \( S \) input.

---

5. The circuits have been designed to allow for the most unfavourable voltages and resistances within the tolerances quoted, and for the transistor data at the end of the operating life; undisturbed operation under full load is guaranteed in the temperature range from \(-10\) °C to \(+50\) °C.

6. Signal tolerances:

- "1" \(\equiv +6 \ldots +12\) V,
- "0" \(\equiv 0 \ldots +1.8\) V.

The two types of block

The active block (fig. 2a) contains a gate circuit with diodes \((D_1 \ldots D_5, R_K, R_B)\), an inverter circuit and a pulse gate \((D, C_P, R_B, R_T)\). The diode gate and the inverter circuit together form a NOR unit, so that the following relationship exists between the output \(C\) and the four inputs \(B_1 \ldots B_4\):

\[
C = B_1 + B_2 + B_3 + B_4.
\]

If desired, the number of inputs can be increased by connecting extra diodes to one of the inputs \(B_1 \ldots B_4\). The operation of the pulse gate will be explained together with that of the counting and memory stages.

The contacts are so arranged (fig. 2b) that even with complicated circuits the connections between the blocks can be made without crossovers (see fig. 5).

The passive block (fig. 3a) contains a gate circuit with diodes and resistors, which gives the following AND relationship between the output \(A\) and the two inputs \(E_1\) and \(E_2\):

\[
A = E_1 \cdot E_2.
\]

The gate resistance used can be either \(R_G\) or \(R_G/2\), or — by combining these resistors in series or in parallel — \(3R_G/2\) or \(R_G/3\), respectively. This gives the passive block a good measure of adjustment to circuit requirements in so far as loading and power consumption are concerned. An AND circuit with more than two inputs can be obtained by connecting the outputs of a number of passive blocks, while connecting the resistance of only one block to the power supply. The arrangement of the contacts is shown in fig. 3b.

Circuits built up of active blocks

The bistable circuit

With the known systems of blocks the counting and memory functions are realized with the aid of various types of bistable circuit, which are varied to suit the different functions required. Sometimes special blocks are provided for this purpose, while sometimes these circuits are built up from two NOR or NAND blocks \([4]\) \([5]\).

The bistable circuit (flip-flop) consisting of the two types of active block is shown in fig. 4a for the asynchronous counting mode and in fig. 4b for the synchronous. In both cases negative switching pulses necessary to block the conducting transistor are applied to the input denoted by \(P\). In the asynchronous method, the pulse gate consisting of the diode \(D\), the resistor \(R_T\) and the capacitor \(C_P\) ensures that the switching pulses can only have an effect at the base of the conducting transistor \([6]\).

In the synchronous method negative pulses are continually applied to the \(P\) input. These only trigger the bistable circuit if the signal "0" (collector potential of a conducting transistor) is applied to the \(S\) input.

---

The logical convention here is thus the opposite of that for the system; this is why we denoted this input by \( \bar{S} \) instead of by \( S \). The signal has to be inverted for each signal input. This is done by an active block which, apart from regenerating the potential, can also serve to carry out the OR operation which is frequently required at this place (see fig. 6). These active blocks may only be loaded with AND circuits.

If negative parasitic pulses occur in the output leads of a bistable circuit, they must be prevented from reaching the base of the conducting transistor via the internal feedback, in which case they could trigger the bistable circuit. This can simply be done by placing an AND gate in each feedback loop (decoupled flip flops)\(^7\). In the circuits described below this is not necessary.

**Polystable circuits**

The new system of circuit blocks can be used not only for bistable but also for polystable circuits with a maximum of five stable states. The number of stable states possible is equal to the number of active blocks used.

In the circuit with five stable states (quinary circuit) (fig. 5a), the output of each of the five active blocks is connected with an input of each of the other four blocks. Since the outputs of the blocks are made double, the connections can be made without crossovers (fig. 5b). One transistor is always cut off, while the other four are kept conducting via the base inputs.
connected with the collector of the cut-off transistor. Triggering is from the central clock-pulse generator via the pulse gates, the potentials at the \( S \) inputs determining which transistor will be marked (cut off).

A quinary circuit can be turned into one with four or three stable states by the omission of one or two blocks respectively, together with those leads which only connect inputs with one another.

**The reversible biquinary decade counter**

A synchronous decade counter can be made very simply by the combination of bistable and quinary circuits \[8\]. Since the biquinary system of counting is very closely related to the decimal — 2 and 5 are the prime factors of 10 — there is no need to modify the circuit to eliminate superfluous counting capacity. This is important, because such modifications are required for both counting directions. The reading-out of the digits is simpler than with the normal decade counters consisting of four bistable circuits. Ten AND circuits (AND gates) with an average of three inputs each are necessary to read ten digits from the positions of the four bistable circuits. In the biquinary counters, however, ten AND gates with two inputs each are sufficient. Fig. 6 shows the logic circuit of a reversible biquinary decade counter, using the coding of Table I.

Before a counting pulse is fed to the circuit, it is first synchronized with the clock pulse, so that its length becomes equal to the interval between two clock pulses. Each counting pulse, for counting both forwards and backwards, prepares the binary stage \( B \), which is then switched over by the clock pulse. The quinary stage must switch over to another position in two situations, viz 1) when the output \( C \) of the binary stage has the potential corresponding to the value “1” and a forward-counting pulse is present, and 2) when the value “1” is found at the output \( C \) of the binary stage and a backward-counting pulse is present. The counting pulses and the

**Table I. Code of a biquinary decade counter.**

<table>
<thead>
<tr>
<th>Digit</th>
<th>Binary stage</th>
<th>Quinary stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( C )</td>
<td>( Q_1 )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

position of the binary stage are combined by the AND gate \( G_V \) for counting forwards and \( G_R \) for counting backwards.

In forward counting, the pulses for the quinary circuit are fed from \( G_V \) to the AND gates \( G_V1 \ldots G_V5 \), and in backward counting from \( G_R \) to the AND gates \( G_R1 \ldots G_R5 \). A pulse which must be counted forwards by the quinary circuit will e.g. pass the AND gate \( G_V2 \).

![Fig. 6. a) Reversible biquinary decade counter. b) Circuit for reading-out of digits from this counter. (The \( P \) inputs of \( B_1, B_2 \) and of \( Q_1 \ldots Q_5 \) must be connected to the common clock-pulse line.)](image)
which is opened by the “1” signal at the output $C_2$ of stage $Q_2$, thus priming the signal input $S_3$ of the next stage (in the forward direction) $Q_3$. Similarly, with a pulse that has to be counted backwards the AND gate $GR_2$ is opened and the next stage (in the reverse direction) $Q_1$ is primed via the signal input. The actual switching-over is always initiated by the next clock pulse to coincide with the counting pulse.

**Special circuits**

A multivibrator can be built up of two active blocks by connecting their outputs $C$ crosswise via capacitors $C_2$ to the direct base leads $B_0$ and by connecting both the leads which are normally intended for the negative and the positive supply voltages to the positive supply voltage.

In the monostable circuit the static coupling — as in the bistable — is formed by the combination $R_K$, $C_K$, $D_1$ and $D_3$. An external capacitor $C_2$, which must be connected between the collector $C$ and the base input $B_0$, determines the delay time. The base bias resistance of the capacitively coupled transistor is connected to the positive supply voltage, so that this transistor conducts in the stationary state. The monostable circuit is triggered via the $P$ input of the capacitively coupled block.

A Schmitt trigger is formed by connecting two active blocks in series, the emitter leads $E$ being earthed via a common resistor. The threshold level can be adjusted by means of another external resistor connecting the direct base lead $B_0$ of the first block with the positive supply voltage. Excitation is via one of the NOR inputs of the first stage.

**Loading rules**

The combination of active and passive blocks to give a logic circuit must be done in accordance with the loading rules, since each block is loaded by the subsequent stages and itself forms a load for the previous stage. Because there are only two types of circuit block, the loading rules can be kept simple.

Each input $B_1 \ldots B_n$ of an active block (NOR) represents a “NOR load” for the previous stage. Each input $E_1 \ldots E_m$ of a passive block (AND gate) represents a certain number of “gate loads” for the previous NOR stage; this number depends on the choice of the total gate resistance:

<table>
<thead>
<tr>
<th>Total gate resistance</th>
<th>$3R_0/2$</th>
<th>$R_0$</th>
<th>$R_0/2$</th>
<th>$R_0/3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of gate loads $k$</td>
<td>$2/3$</td>
<td>$1$</td>
<td>$2$</td>
<td>$3$</td>
</tr>
</tbody>
</table>

These two types of load may not be discounted against one another when calculating the maximum permissible load.

With a few exceptions, which cannot be discussed within the scope of this article, the following simplified loading table is obtained (where allowance must still be made for the restriction mentioned on page 167 for the NOR circuit for signal inversion at the $S$ input of a bistable circuit):

<table>
<thead>
<tr>
<th>Previous stage</th>
<th>Type of load</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOR</td>
<td>AND</td>
<td>$g \leq 8; \sum k \leq 8$</td>
</tr>
<tr>
<td>NOR</td>
<td>NOR</td>
<td>$n \leq 4$</td>
</tr>
<tr>
<td>AND</td>
<td>NOR</td>
<td>$n \leq k$</td>
</tr>
</tbody>
</table>

Here $g$ is the maximum number of gate loads which can be carried by a NOR stage (gate loads must be added, no matter whether the AND gates are connected in parallel or in series), $k$ is the number of gate loads corresponding to an AND gate, and $n$ the maximum number of NOR loads that can be carried by the previous stage.

Fig. 7 shows a possible realization of a NOR block

![Fig. 7](example.png)

Fig. 7. Examples of the construction of two circuit blocks, as used e.g. in electronic weighing installations. Above AND circuit, centre and below: NOR circuit.

---


and of an AND block. In order to increase the economy of this system, these two types of block can be supplemented by another active block consisting of two NOR circuits without pulse gate. These can be used with advantage wherever the NOR does not form part of a bistable or polystable circuit.

Fig. 8 shows a reversible biquinary decade counter with 10 output amplifiers for the digits 0...9.

The system of circuit blocks described here has been used in electronic weighing installations with digital data encoding and processing.

The synchronous biquinary decade counter was developed by P. Muuss of the Hamburg Laboratory.

**Summary.** This paper describes a new system of digital circuit blocks, designed to meet the special needs of industrial measurement and control techniques, characterized by the following:

a) It contains only two different basic circuits: an active logic circuit in diode-transistor logic (DTL), and a passive logic circuit in diode logic.

b) It contains only one type of transistor and two types of diode; there are no emitter-followers.

c) The basic circuits of this system can be combined to give not only bistable but also polystable circuits with for example 3, 4 or 5 stable states.

d) The bistable circuits can be used for either the synchronous or the asynchronous counting mode.

e) The circuit blocks operate reliably under full load in the temperature range from $-10^\circ C$ to $+50^\circ C$ with the most unfavourable values of the resistances and voltages within their tolerances, and with the smallest current amplification and the greatest leakage currents which can occur at the end of life of the transistor.

f) The loading table is simple.

g) Special circuits, such as multivibrators, monostable circuits as well as Schmitt triggers, can be realized by simple combination of two active blocks and one or two extra resistors or capacitors.

---

**Generation of musical intervals by a digital method**

D. Gossel

534.321.2:621.389

**Introduction**

The familiar kinds of musical instrument can be divided into two classes:

a) Instruments producing notes whose pitch is not decided upon until the instant of playing: bowed string instruments and certain wind instruments are examples.

b) Instruments possessing a store of notes, from which in the course of playing a selection is made in accordance with a programme. All keyboard instruments belong to this class.

Instruments in class (b) can only be endowed with a limited store of notes for constructional reasons, and because the technique of execution might otherwise be rendered too difficult; also, the access time for whatever notes are available must be compatible with practical requirements for playing the instrument. This implies the existence of some fixed rule or instruction for selecting individual tones from the continuum of pitch.

Several such rules have been laid down at various times in the history of music [1], they find practical expression in the various tonal or tuning systems. The four most important will now be briefly explained and discussed.

**Tonal systems**

A tonal system has been defined [2] as a scheme for dividing the octave into a progressive sequence of tones, the principle underlying the division being consistently adhered to and designed to produce musically acceptable intervals.

1. Pythagorean tuning

This system dates back to the philosopher who lived during the 6th century BC. It is based upon the fifth,